Flexible and Transparent Silicon-on-Polymer Based Sub-20 nm Non-planar 3D FinFET for Brain-Architecture Inspired Computation

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Silicon electronics are at the heart of today's digital world. Silicon based electronics have unparalleled performance, cost and yield advantage, making it the most preferred material for ninety percent of digital electronics. Still, ultra-mobile high performance computation capabilities are yet to be achieved. Human brain is the role model to achieve that goal, as it is the world's most powerful, energy efficient and compact natural computer. Interestingly human brain is not rigid or brittle as silicon. The human brain is compact, so the design is based on folded layers to enhance the functionality in an ultra-compact area. In that regard, exploration for a low cost simple solution using plastic as substrate and organic materials to fabricate electronics, like displays and sensors, is on rise.[1–4] They are widely known as flexible electronics. Although organic electronics have already proved their usefulness in commercial flexible LED displays,[5,6] their thermal instability and inherently low electron mobility[7] hinder their potential for truly high performance computing applications. On the other hand, very high mobilities (10^3 cm^2 V^{-1} s^{-1}) have been recently demonstrated with aligned arrays of single-walled carbon nanotubes (SWCNTs) and atomic crystal structure graphene.[8,9] However, the techniques used in the fabrication of medium-scale circuits using SWCNTs[10] are not feasible for integration in process technologies such as silicon semiconductor processing. In the case of graphene, its nearly zero band-gap semi-metallic property limits its potential for digital application due to the lack of clearly distinguishable on/off behavior, making it more suitable for radio-frequency (RF) applications. Recently, extraordinary progress has been championed by JA Rogers et al. to combine the outstanding mechanical and electrical properties of silicon with the flexibility offered by polymer based substrates.[11–28] Extremely high-resolution mask alignment is a long-established task in today's semiconductor industry for the fabrication of ultra-large-scale circuits and yet, it is not possible in plastics due to limited flatness and uniformity of the substrate. For this reason, an alternate approach of fabricating devices first and thinning down the silicon substrate to achieve flexibility has recently been investigated. This methodology consists of polishing, grinding and thinning-by-dicing.[29,30] However, these thinning techniques make use of abrasive processes that may damage the on chip devices while trying to achieve a few tens of microns in thickness to obtain good bendability further reducing the yield and hence eliminating one of the major advantages of silicon fabrication technologies, high cost/yield. Recently, a new technique has been developed to produce thin substrates out of standard wafers by exfoliation or spawlling processing.[31,32] The use of extremely costly substrates, limited bendability and opaqueness of the released portion are the major problems with this technique. Another technique explored to create high quality single-crystal silicon films consist of creating a double layer of silicon and introducing porosity in the bottom layer with anodic etching.[33,34] Although highly complex circuitry has been demonstrated with this technique, the introduction of unfamiliar procedures such as anodic etching makes it difficult to integrate it with modern fabrication processes. Also, the high processing costs and complexity associated with silicon epitaxy as well as limited bendability and opaqueness hinders its potential for low-cost/high-yield applications. Finally, commercially available flexible and thin substrates are an alternative to overcome all previous drawbacks, but they come with a higher cost and handling difficulties due to their extreme fragility, making them unsuitable for standard industry processes.

To address all these concerns, in the recent past we have demonstrated transformational electronics, where we transform the traditional silicon electronics into flexible and transparent ones with already fabricated devices retaining their status-quo performance, efficiency, ultra-large-scale-integration density, thermal budget and finally cost.[35–38] Following a modified process, here we demonstrate for the first time flexible and transparent devices using semiconductor industry's most advanced architecture and material set: FinFET high-κ/metal gate stacks. FinFET is a new generation device architecture which has been adopted by semiconductor giant Intel Corporation from 2011 in their microprocessors.[39,40] FinFET, a member of multi-gate FET family, offers non-planar 3D topology where the channels are vertically aligned in arrays of ultra-thin silicon fins bordered by multiple gates (in our case it is two gates) to ensure higher electrostatic control to mitigate short channel effects as well as enhance performance (**Figure 1**a). In addition to the advanced topology, we have also integrated semiconductor industries'

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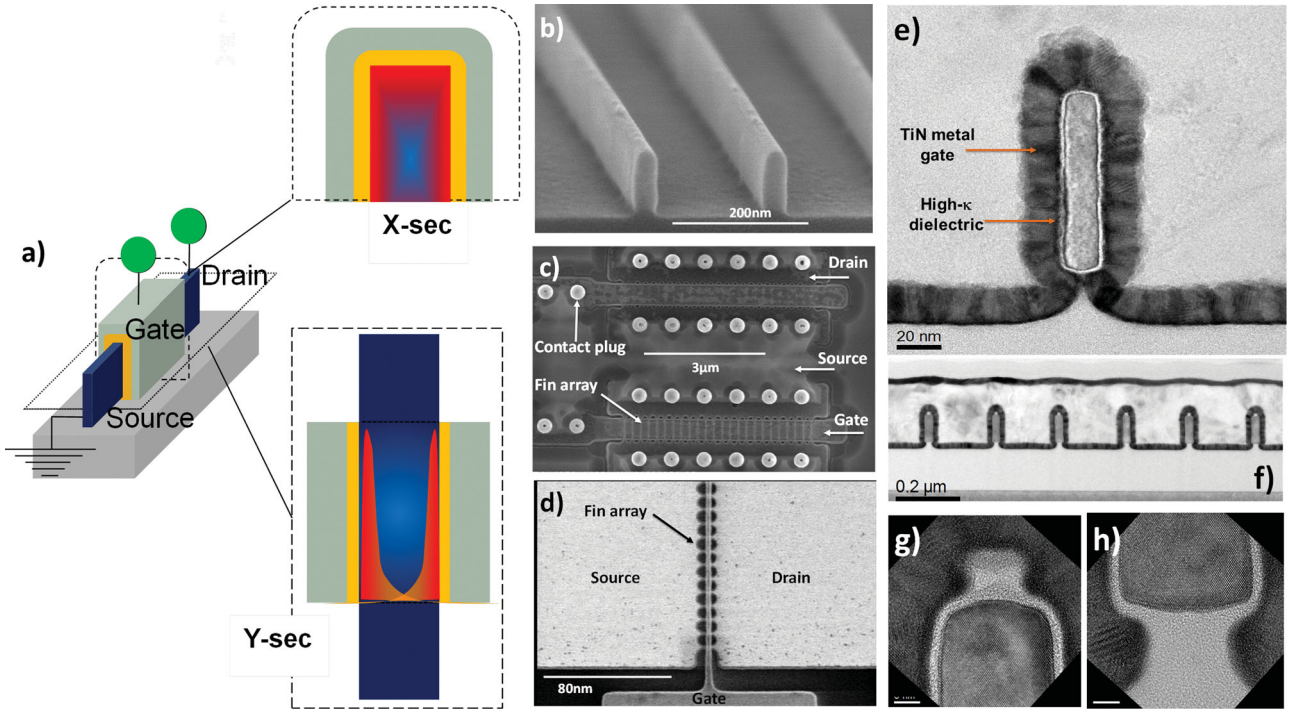

Figure 1. Fabrication process flow of p-type MOSFET on Si (100) fabric. Detailed description is in the main text. FinFET physics and physical imaging: a) FinFET is a non-planar 3D device architecture conceptualized by Prof. Chenming Hu (University of California at Berkeley) and commercially marketed by Intel Corporation from 2011. Tri-gate has vertically oriented channel wrapped around by gates from 3-sides (FinFET has gates from 2-sides) achieving ultra-thin-body channels trending towards volume inversion for higher drive current and better electrostatic control with multiple gates for short channel effects mitigation resulting in controlled leakage power consumption. The zoomed in images show electron distribution under bias conditions. Here, surface inversion charge densities interact with each other from the opposing and adjacent sides leading to orders of magnitude lower leakage current in ultra-short channel devices (<22 nm) and near ideal sub-threshold swings. b) Tilted images from SEM of arrays of fins after fin patterning and smoothening of the sidewall process. c) Top view of fabricated fins showing arrays of fins, source-drain-gate and contact plugs. Since fins are ultra-thin like nanowires, they have to be arrayed for appreciable amount of current. d) Top view of fins after gate etch process, which is a complex task performed with a combination of reactive ion etching and wet cleans. e) A transmission electron microscopic (TEM) image of cross-section of an individual fin showing 13 nm width and 88 nm height. f) TEM image of array of fins on buried oxide (125 nm). g and h) TEM images of top and bottom portion of a fin showing conformal deposition of ALD based gate-stacks. Scale bar in figures e and f is equal to 5 nm.

most advanced high-κ/metal gate stacks to make our device fully state-of-the-art. The devices show extra ordinary high performance. Additionally, this is the first time we effectively eliminate the scallops at the bottom of the silicon fabric due to the presence of buried oxide layer (BOX). Finally, we have transferred our devices on flexible silicon fabric to another flexible platform: polymer. From all these perspectives, this work is the significant advancement for flexible inorganic high-performance electronics, a step forward for physical modeling of brain-architecture inspired computing.

The FinFET P- and N- MOS fabrication process can be found in previous work[40] as well as in the supporting information. The FinFET architecture, scanning electron and transmission electron microscopic images are shown in Figure 1(b-g). **Figure 2** shows the basic steps to release FinFETs from the carrier substrate and transfer them to a polymer substrate. Each of the fabricated wafers was diced into 2.5 cm × 3 cm pieces in order to process each die separately. At this point, dies were processed with research level lithography to create the etch hole patterns in the inactive areas of the fabricated devices (Figure 2b). The distance between the holes depends on the selectivity of the isotropic etchant between silicon and buried oxide (BOX) (>1000:1) and the thickness of the bottom oxide layer. The next step consists of removing the interlayer dielectric (ILD) from the holes to allow access for xenon di-fluoride (XeF_2) isotropic etchant. Next, while keeping the photoresist, the dies were placed in XeF_2 chamber to isotropically remove the silicon from the bottom of the BOX and create caves (Figure 2c). Once these caves meet with each other, the SOI and the BOX is completely released from the bulk substrate allowing us to peel-off the devices (Figure 2d) and transfer them to a flexible polyimide carrier substrate (Kapton) with a thin uncured polydimethylsiloxane (PDMS) spin coated film to enhance adhesion between the peeled devices and the carrier substrate (Figure 2e). Finally, the PDMS layer is cured. It is to be noted that the holes did not represent any constraint in the design of the fabricated devices due to high selectivity between thermal oxide and silicon under XeF_2 etching conditions. The yield rate of fabricated unreleased device is nearly 75% (which is consistent with our previous publications[35,36]) out of 1000 fabricated devices. We had a transfer yield of approximately 80%. The devices which did not yield are due to slicing and dicing the silicon fabric. So, the data collected are from 600 devices.

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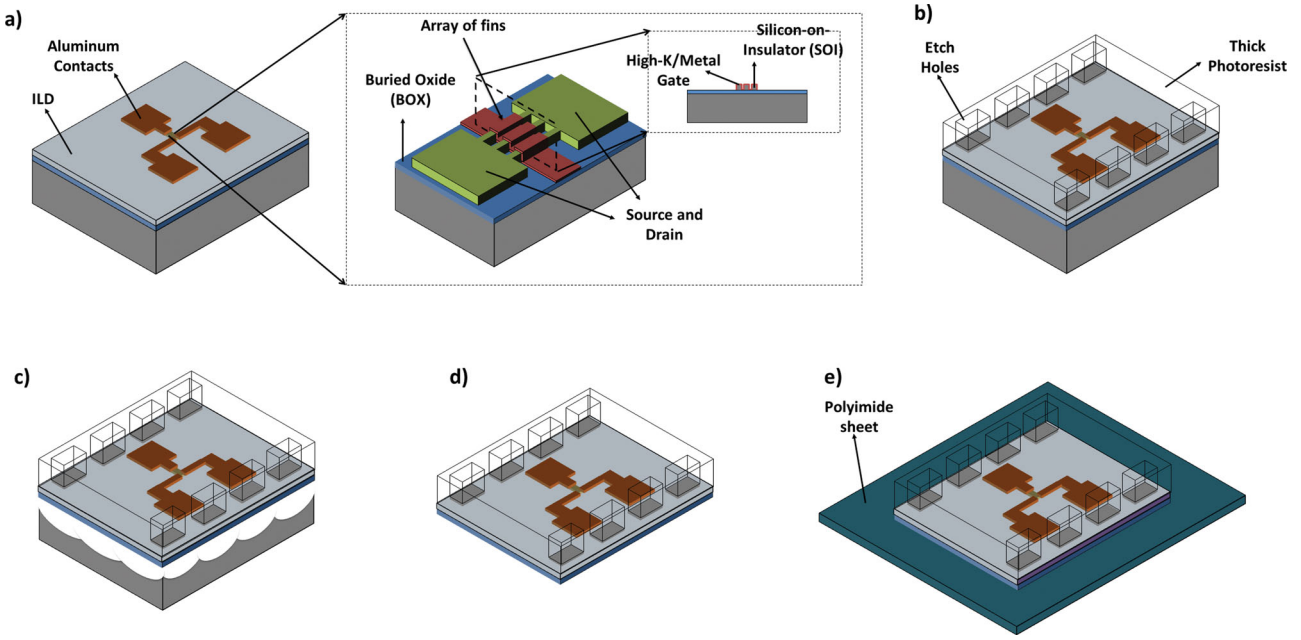

Figure 2. Schematic flow for silicon fabric release containing FinFETs. a) Initial FinFET device fabricated on 90 nm thick SOI, aluminum contact pads and 850 nm ILD. Projection: FinFET channel, source and drain and gate stack, b) Spin coat of thick (7μm) photoresist and hole patterning, c) Cavern formation beneath BOX due to XeF_2 etchant, d) Released fabric (1 μm) after 600 cycles in XeF_2 isotropic etchant, e) Transferred devices to 125 μm thick polyimide sheet spin coated with thin PDMS adhesion layer (≈1 μm).

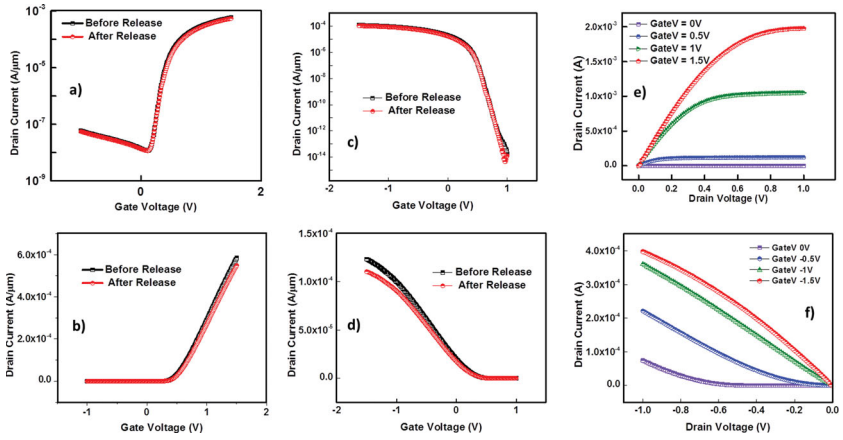

Figure 3. Electrical characteristics comparison between P- and NMOS devices on before and after release silicon fabric (L = 250 nm, W = 3.6 μm, C_{ox} = 41.3 fF/μm^2, V_{ds} = 1 V). a) I_D-V_G transfer characteristics in logarithmic scale for NMOS. b) I_D-V_G transfer characteristics in linear scale for NMOS. c) I_D-V_G transfer characteristics in logarithmic scale for PMOS. d) I_D-V_G transfer characteristics in linear scale for PMOS. e) I_D-V_D curves for NMOS. f) I_D-V_D curves for PMOS.

To study the behavior of the FinFETs, we first measured the transfer (I_d-V_g) characteristics. **Figure 3** (a–d) shows a comparison for the same PMOS and NMOS devices before and after peel-off processing. The measured NMOS and PMOS devices have gate length (L) 250 nm and channel width (W) 3.6 μm. The current at saturation with V_{GS} = 1.5 V for NMOS and V_{GS} = –1.5 V for PMOS at V_{DS} = 1 V and –1 V respectively are 549 μA/μm (standard deviation = 13.96 μA/μm) for NMOS and 110 μA/μm (standard deviation = 2.88 μA/μm) for PMOS, and 58.48 μA/μm (standard deviation = 1.52 μA/μm) and 7.73 μA/μm (standard deviation = 0.21 μA/μm) at V_{DS} = 50 mV and –50 mV for NMOS and PMOS, respectively. In the case of NMOS, I_{on}/I_{off} ratio is 4.6 decades and for PMOS is 4.78 decades. I_{on}/I_{off} ratio was calculated using Intel Corporation's method, which states that I_{off} should be calculated at V_{th} minus one third of V_{DS} for non-optimized gate stacks.[41] Gate leakage was found to be 3.6 A/cm^2 (standard deviation = 0.095 A/cm^2) for NMOS and 1.18 A/cm^2 (standard deviation = 0.03 A/cm^2) for PMOS at V_{GS} = 1.5 V and V_{GS} = –1.5 V respectively. The electrical characterization started by extracting the saturation threshold voltage (V_{th}^{sat}) from the I_D-V_G curve using linear extrapolation method.[42] From the I_D-V_G curves, the threshold voltage is determined by:

$$V_{th}^{sat} = V_{GS_0} - \frac{V_{DS}}{2} \quad (1)$$

Where, V_{GS_0} is the intercepting point from the linear extrapolation in the I_D-V_G curve. From Equation (1) the obtained saturation threshold voltage for NMOS is 0.345 V and for PMOS is 0.713 V. Mobility was extracted at low drain voltages by:

$$\mu_{eff} = \frac{L}{W} \frac{g_d}{C_{ox}(V_{GS} - V_{th}^{sat})} \quad (2)$$

Where, V_{GS} and V_{th}^{sat} are the gate to source voltage and threshold voltage respectively, C_{ox} is the gate oxide capacitance,

L and W are the gate length and width respectively, and g_d is the drain conductance determined by:

$$g_d = \frac{\partial I_{D\_eff}}{\partial V_{DS}} | V_{GS} = \text{constant} \quad (3)$$

Where I_{D_eff} is the effective drain current when gate leakage is taken into account. When extremely thin dielectrics are used, as in this work (Hafnium based high-κ dielectric thickness = 30 Å), gate leakage opposes the drain current and reduces the drain conductance, hence reducing the μ_{eff}. I_{D_eff} is determined by:

$$I_{D\_eff} = I_D + \frac{I_G}{2} \quad (4)$$

With Equations (2), (3) and (4) the effective mobility was estimated to be 141.53 $cm^2\ V^{-1}\ s^{-1}$ (standard deviation = 3.74 $cm^2\ V^{-1}\ s^{-1}$) for NMOS and 13.22 $cm^2\ V^{-1}\ s^{-1}$ (standard deviation = 0.35 $cm^2\ V^{-1}\ s^{-1}$) for PMOS. Non-optimized gate-stacks resulted into lower PMOS mobility. The work function of TiN as deposited is 4.4 eV, which is not suitable for PMOS transistors, this causes the devices to have a lower transconductance (g_m) and hence a reduced hole mobility. This can easily be solved with metal gate tuning for P- and N- MOS devices which is not within the scope of the manuscript.[40] However, it is to be noted that although the mobility for PMOS devices is low, it is not affected by the release or transfer process, further showing the consistency of our process for both N- and P- MOS. Finally, the sub-threshold swing (*S*) was extracted from the slope in the I_D-V_G curve when plotted in a logarithmic scale. From Figure 3a, sub-threshold swing (*S*) is obtained as 80 $mVdec^{-1}$ for NMOS and 70 $mVdec^{-1}$ for PMOS, showing that the FinFETs have extremely fast switching actions. As can be observed, there is a small current reduction of 7% for NMOS and 12% for PMOS in the saturation region of the transistors. Once the sample has been released from the bulk, the amount of residual strain contributed by the inter-layer dielectric (ILD) becomes much more significant as previously reported in past work[44] and hence reduces the on state current. In the case of I_{off}, there is no significant change when comparing the released and in-bulk devices. This is due to the complete isolation that SOI wafers provide between the carrier substrate and the active part of the transistor. I_{off} for released and unreleased NMOS was found to be 13.79 nA/μm (standard deviation = 0.39 nA/μm) and 15.63 nA/μm (standard deviation = 0.34 nA/μm) respectively and I_{off} for released and unreleased PMOS was found to be 1.82 nA/μm (standard deviation = 0.09 nA/μm) and 3.54 nA/μm (standard deviation = 0.046 nA/μm) respectively. V_{th}^{sat} for released and unreleased NMOS was 0.325 V (standard deviation = 0.009 V) and 0.345 V respectively and V_{th}^{sat} for released and unreleased PMOS was 0.66 V (standard deviation = 0.018 V) and 0.713 V, respectively. The difference in V_{th}^{sat} does not represent a significant change (only 6% for NMOS and 8% for PMOS), therefore confirming the consistency of the process. The comparison between sub-threshold swing for released and unreleased samples also indicates an insignificant change of only 3.4% for NMOS and 2.8% for PMOS. In summary, apart from the 7% for NMOS and 12% for PMOS reduction in the "ON" state current, the devices behave very similarly when comparing released NMOS and PMOS with unreleased NMOS and PMOS. It is to be noted that PMOS devices were not optimized for V_{th} during the fabrication process. This causes a large shift of V_{th} towards the positive side of the gate voltage; however, the difference between released and unreleased PMOS devices differ in only 8% of the original threshold voltage value, showing the consistency of the release process.

To start the mechanical characterization of the released devices, the maximum applied strain at which silicon is subject to fracture stress[43] was calculated to be 13% with Equation (5).

$$\sigma = E\varepsilon \quad (5)$$

Where σ is the fracture stress limit, E is the Young's modulus for (100) single crystal silicon and ε is the applied strain. The minimum-bending radius in device scale was obtained by checking the performance of the released devices until the point cracks in any of the device stack materials causing extreme degradation in the performance. Due to the extremely small thickness of the released substrate (≈ 1 μm), high bendability is achieved while keeping the device performance almost unaltered. The minimum-bending radius was found to be 5 mm (**Figure 4**a) and thus

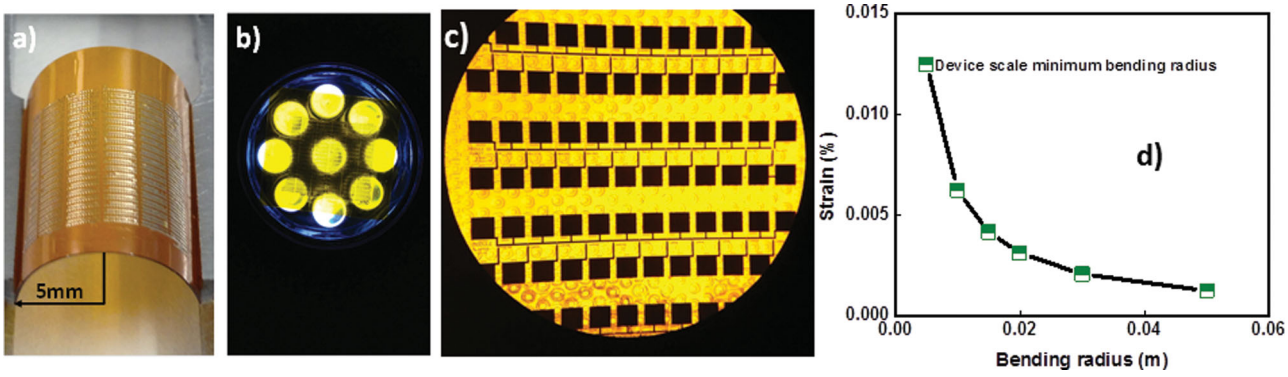

Figure 4. a) FinFET silicon fabric at minimum device scale bending radius (5 mm). b) Transparency through the flexible silicon with devices, placed on top of a torch. It is to be noted that the fabric is not rolling back rather staying as it is placed without any adhesive or force. c) Optical microscopic image of released devices. d) Nominal strain calculation for different bending radius (50, 30, 20, 15, 10, 5 mm).

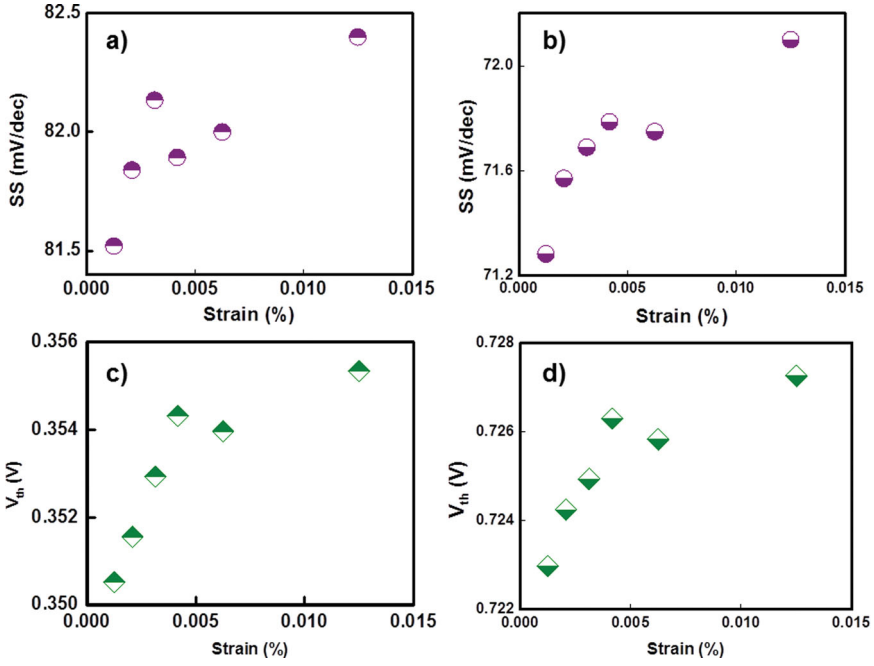

Figure 5. Device performance dependence on applied nominal strain. a-b) Threshold voltage (V_{th}) behavior under different strain conditions. c-d) Sub-threshold slope (*SS*) behavior under different strain conditions.

electrical characterization was also done up to this limit. We also show the transparency of the devices (Figure 4b), and optical microscopic images of the released devices (Figure 4c). Bubbles in this image are trenches. In order to characterize the device performance at different bending radius, the devices were electrically tested at different nominal strain values (Figure 4d) calculated from:

$$\varepsilon_{nom} = \frac{t}{2R} \tag{6}$$

Where t is the thickness of the fabric and R is the bending radius. At 5 mm, the top surface of the fabric is subject to 0.0125% strain in the longitudinal direction of the transistor's channel, in the case of FinFETs, parallel to the longitudinal direction of the patterned Fins. **Figure 5** shows the electrical behavior of the devices at different applied strain levels. The electrical characterization set-up for measuring the device performance was set at different bending radius (5, 10, 15, 20, 30 and 50 mm). Sub-threshold slopes are true indicator of the fast switching in transistors, therefore we studied them critically and found the difference between bent and non-bent devices was only 3% for NMOS and 3% for PMOS (Figures 5a and b). Standard deviations of SS (NMOS) are 2.04, 2.11, 2.1, 2.1, 2.1, 2.1, 2.09 mV dec^{-1} and SS (PMOS) are 1.80, 1.85, 1.85, 1.85, 1.85, 1.84, 1.84 mV dec^{-1} for flat, 50, 30, 20, 15, 10 and 5 mm bending radius, respectively. We also observed (data not shown rather discussed) that I_{off} increases with the strain while I_{on} decreases. It has to be noted that although device performance is degraded proportionally to the amount of strain, the changes are still negligible at maximum strain, showing only 10% for NMOS and 9% for PMOS increase in I_{off} and 11% for NMOS and 8% for PMOS decrease in I_{on}. In Figures 5(c and d) in the case of V_{th}, the difference between bent and non-bent devices is merely 3% for NMOS and 2% for PMOS. Standard deviations of V_{th} (NMOS) are 9.1, 8.9, 8.8, 8.5, 8.8, 8.8, 8.8 mV and V_{th} (PMOS) are 18.4, 18.8, 18.8, 18.8, 18.8, 18.7, 18.7 mV for flat, 50, 30, 20, 15, 10 and 5 mm bending radius, respectively. Finally, the results concur with previously reported studies[38,44] where, values for reduction in saturation current are shown for longitudinal strain applied to the channel of the transistors.

We have demonstrated a pragmatic way to transform SOI based state-of-the-art FinFET into flexible and semi-transparent silicon-on-polymer FinFET while retaining high performance and integration density. The process shown has the unique characteristic that all the devices can be fabricated prior to release without any constraint set by the high thermal budget or by the etch holes due to the extremely high etch selectivity between silicon and silicon dioxide. Our process thus sets a major step towards the integration of state-of-the-art high performance devices for ultra-mobile brain-inspired foldable computers or ICs. The electrical superiority achieved with inorganic semiconducting substrates and the maturity of silicon microfabrication industry make the integration of silicon on flexible platforms the most logical next step towards achieving high computational capabilities in mobile devices. Ultra-thin (1 μm) nature of the silicon fabric with devices makes it ultra-light-weight also. We have chosen to demonstrate high performance P- and NMOS devices in flexible silicon fabric to prove the compatibility of our process with the backbone of high performance CMOS based electronics. Although we have not shown complete circuitry on flexible silicon fabric due to mismatched V_{th} shift in PMOS devices, this work indicates that with the correct process optimization and integration of dual high-κ/metal gate for threshold voltage correction, we can transform large scale state-of-the-art high performance circuitry without affecting its performance. The released transistors feature the most advanced architectures used in semiconductor industry as well as the most sophisticated set of materials, high-κ/metal gate stack, used to overcome scaling problems in modern solid state devices. Electrical characterization of our devices shows a sub-threshold swing of 80 mVdec^{-1} for NMOS and 70 mVdec^{-1} for PMOS and I_{on}/I_{off} ratio of 4.6 decades for NMOS and 4.78 decades for PMOS. The step sub-threshold swings indicate faster switching with sufficient distinction between on and off state. The released fabric is 1 μm in thickness and is capable of achieving a minimum-bending radius of 5 mm in device scale. Also, since the fabric is extremely thin and our host substrate is a polyimide sheet, the complete set of devices exhibits semitransparency. These fabricated devices show competitive electrical behavior and outstanding bendability relying only on mature microfabrication

processes. Finally, we believe our process sets a major step towards the integration of the most reliable and broadly used material in semiconductor industry, silicon, on flexible platforms for the expansion of ultra-mobile high performance flexible electronics which will mimic ultra-compact brain-inspired folding capability.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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